S1.26 2D MoS_2 Transistors

MARC2024: Microsystems Annual Research Conference

Bianca Hanly, Lucas Ospina, Sanjay Seshan, Dip Joti Paul PI: Farnaz Niroui

Electrical Engineering & Computer Science, Massachusetts Institute of Technology, 6.2540 Course Project

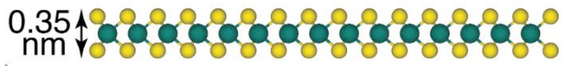
Introduction

Background:

- Approaching the end of Moore's law
  - Shrinking traditional silicon transistors to improve performance is getting harder because of quantum tunnelling
- 2D materials
  - Diverse functionality
  - Better electronic properties
  - Allow for flexible form factors

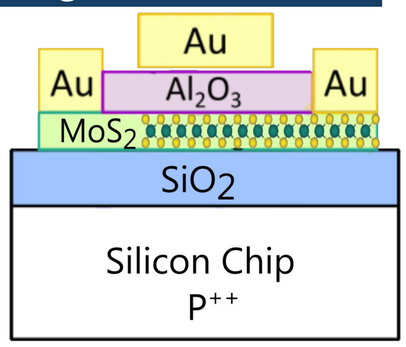
Goal:

- Fabricate a MOSFET using MoS_2 instead of Si
- Implement a top-gate approach
- Characterize transistor performance



Design

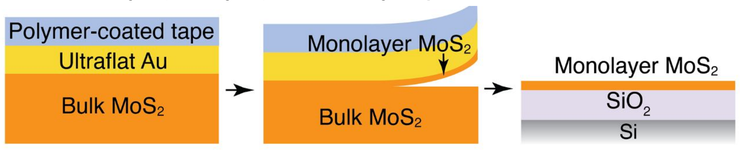
- Silicon base
- MoS2 channel
- Al_2O_3 oxide
- Gold electrodes and traces
- 20 nm and 30 nm oxide thickness
- 3um channel length
- Vary channel width

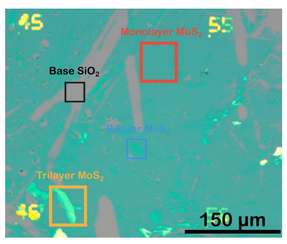


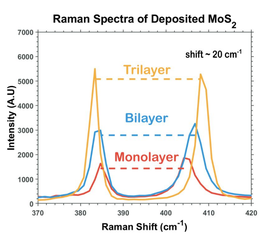
MoS2 Transistor Fabrication

Gold-Mediated MoS2 exfoliation

- Van Der Waals interactions from special polymer is good for picking up large monolayer patches
- Contiguous patches ~100um in each dimension
- Monolayer, Bilayer, and Trilayer patches

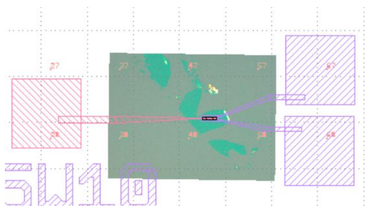


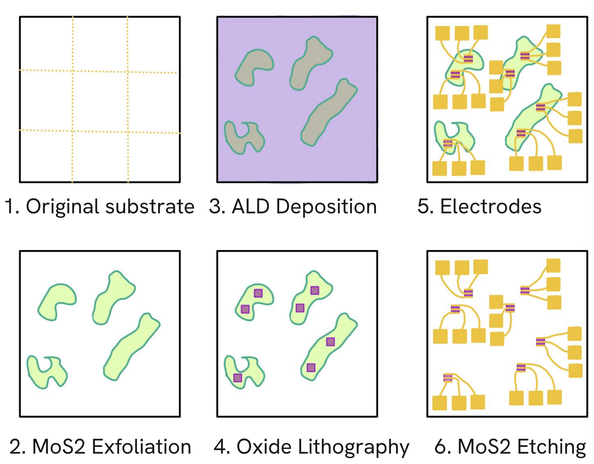




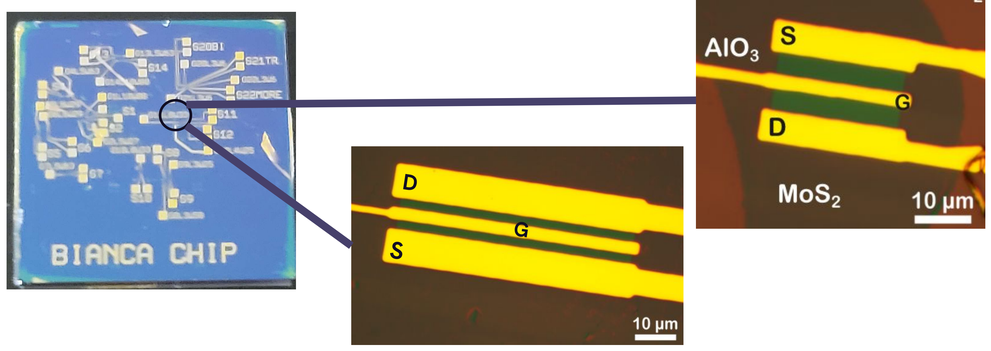
KLayout to generate Lithography Masks

- 1.5um oxide tolerance
- 2um source/drain and gate distance
- 20um traces
- 300x300um contact pads

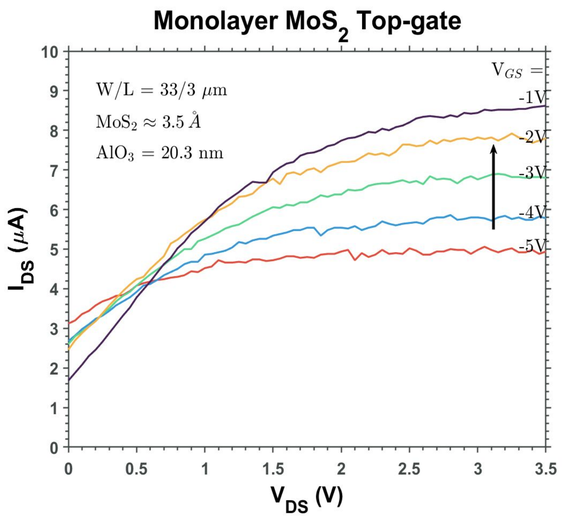




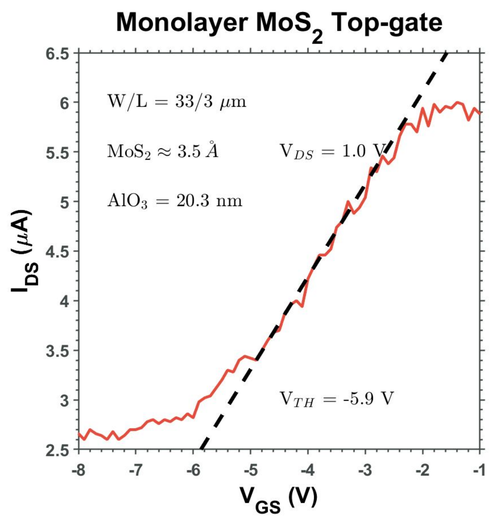
Results

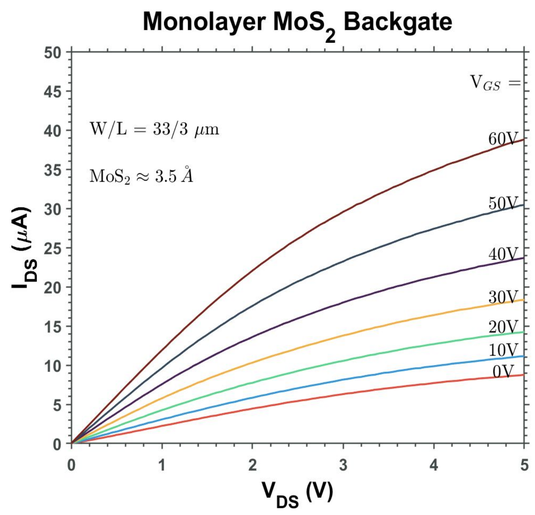


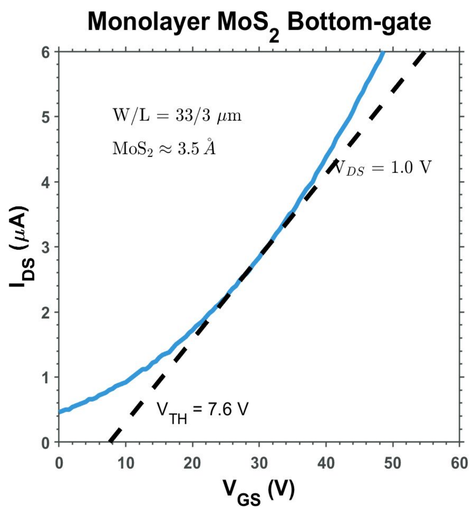
Output Characteristic

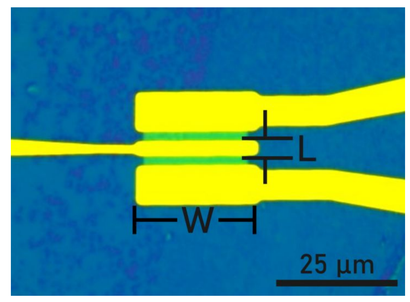


Transfer Characteristics









Theoretical Topgate Saturation Current

$$V_T = V_{FB} + 2\psi_P + \frac{1}{c_{ox}}\sqrt{2\epsilon_s q N_D (2\psi_P)}$$

$$c_{ox} = \frac{\epsilon_o x}{t_{ox}}$$

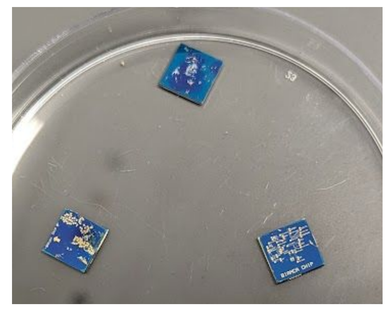
$$= 7.3 * 8.85 * 10^{-12}/(20 * 10^{-9}) = 0.0032$$

$$I_{ds} = \mu_{sat} c_{ox} \frac{W}{2L}(V_{TH} - V_{GS})^2$$

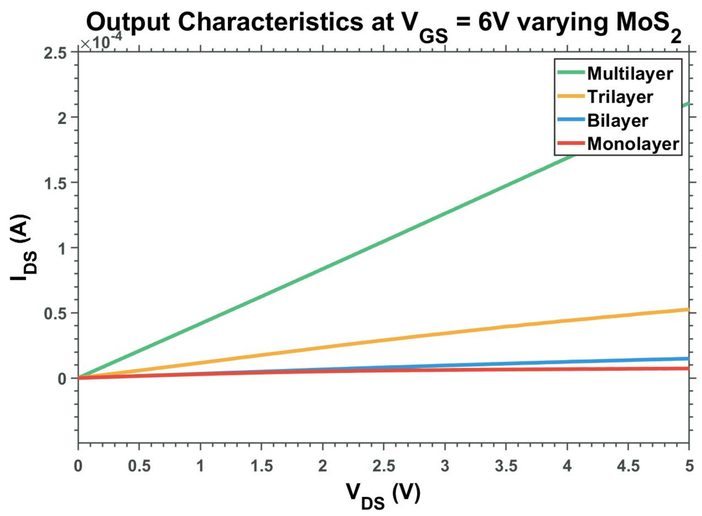
$$= 105 * 0.0032 * 33/6 * (V_{GS} - (5.9))^2$$

For V_{GS} =-1 V -> 44 A
For V_{GS} =-4 V -> 6.7 A

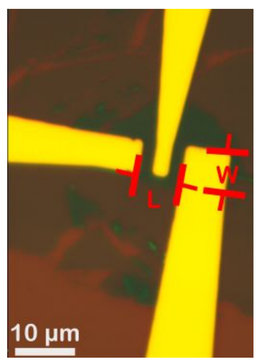
- We had dozens of transistors across 4 chips
  - Presented are samples from chip B
- Back gate and Top gate results are as expected for an NMOS transistor
- Threshold voltages are calculated and drawn on the graphs
- Results are very promising



Multi-layer MoS2

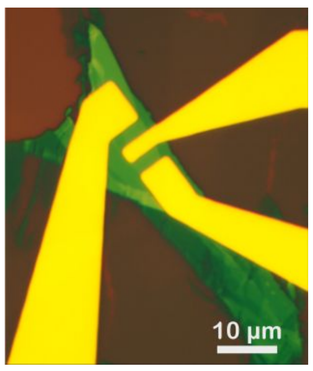


Bi-Layer



Tri-Layer

Multi-Layer



Acknowledgements

6.2540 Staff

MIT.nano

MIT EECS

Special thanks to Sarah Spector and Farnaz Niroui for their contributions

References

- Radisavljevic, B., Radenovic, A., Brivio, J. *et al.* Single-layer MoS_2 transistors. *Nature Nanotech* 6, 147–150 (2011). https://doi.org/10.1038/nnano.2010.279
- Gold mediated MoS2 figure from S1.15 of last years conference
- All other figures are drawn or generated by the authors