An Exploration and Characterization of Digital Logic Using Thin Film Transistors

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***Abstract*—In this paper, we present the usage of Thin Film Transistor (TFT) technology technology to build digital logic systems. Traditionally, TFTs are used as display controllers for LCD since they are easily scalable and can be build on glass substrates, allowing for a strong backlight. However, they are not often used in digital logic systems due to having slower performance compared to MOSFETs or FinFETs (few MHz vs few GHz). TFTs do have strong potential in digital systems, due to their flexibility – we can build TFTs on flexible substrates or for large area ICs. We experiment using these devices to create and test the following circuits: NAND, NOR, and NOT gates. We also construct individual devices for evaluation. With only n-type devices, we construct resistor-transistor logic (RTL)-based circuits with large pull-up resistance. We present promising results for the performance of TFTs in digital logic gates.**

***Index Terms*—nanotechnology, thin-film transistors, devices, integrated circuits**

I. Introduction

Traditionally most computational devices that use logic gates make use of metal oxide semiconductor field effect transistors (MOSFETs) due to their smaller size and generally faster operation. An advantage of TFTs however is that they can be constructed on top of a larger variety of surfaces than MOSFETs, including glass, which is why TFTs are usually used in display technologies. However, TFTs have different characteristics compared to MOSFETs, mainly slower switching and more leakage, which make them traditionally undesirable for high performance compute [1], yet the versatility of these devices make them worth exploring.

In recent years Moore's law is coming to an end [2] with transistors count per chip per year starting to flatten out, which provides a frontier of research for computational engineering. A related trend that was Dennard scaling which described the scaling of transistors halving every few years. This trend ended around 2010, causing electrical engineers to have to explore other methods to improve performance and energy efficiency of devices [3]. We explore new ways to expand computational systems particularly with TFTs which can uniquely find use in large area electronics, flexible, and transparent substrate systems [4] [5].

We design TFT-based circuits using resistor-transistor logic (RTL) in order to create logic gates, NOT (Inverter), NOR, NAND, and XOR whose schematics are shown in Figure 1. These gates are combined to create a flip flop. RTL uses a relatively large pull-up resistance, with a N-type transistor logic to create digital logic without a p-type complementary gate (CMOS).

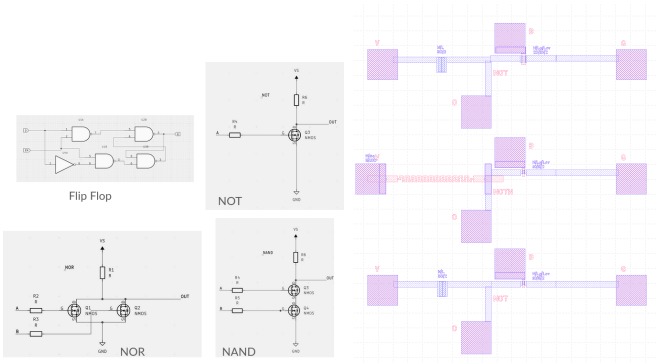

Fig. 1. Schematics and sample layout of our test circuits.

II. Methods

In this section, we will describe how design and test our integrated circuits.

A. Fabrication

We show an overview of our process in Figure 2. We start by depositing 300 nm of SiO_2 by tube oxidation. We then sputter 10 nm of tungsten, and after patterning with photolithography we dry plasma etch the pattern into the tungsten. Next we deposit 15 nm of Al_2O_3 through atomic layer deposition (ALD).

To create connections between the tungsten and nickel-gold layers we create channels using photolithography patterning then etching of Al_2O_3 [6]. We then sputter 3 nm of indium tin oxide (ITO) to create the semi conducting channel.

Finally, we use a liftoff technique by first patterning photoresist then we deposit 30 nm of nickel-gold alloy by evaporation, then remove the unwanted nickel-gold with the photoresist.

When creating TFTs, we created devices with varying channel widths and lengths. These metrics range from 10 um to 50 um in width and 5 um to 20 um in gate size. We evaluate performance when sweeping the gate-to-source voltage (V_{dd}) [7] compared to input V_g to output voltage V_{out}. We compare these metrics to ideal transistor behavior and visually identify values for V_T and the gain.

B. Designs and Testing

The next step in our characterization process is testing various logic gates. We created three types of logic gates for evaluation: NOT, NAND, and NOR. As the simplest of the three, NOR, we created many of these gates with various

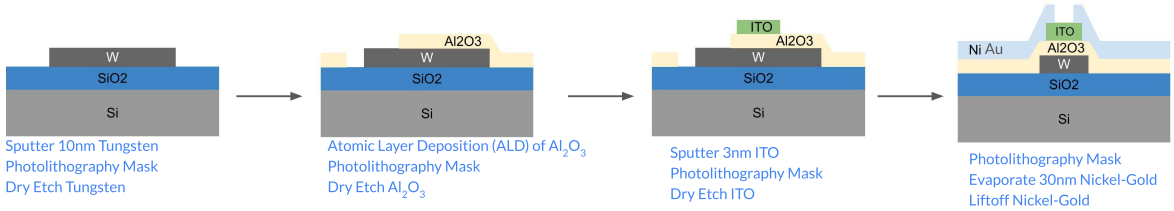

Fig. 2. Overview of the TFT fabrication process.

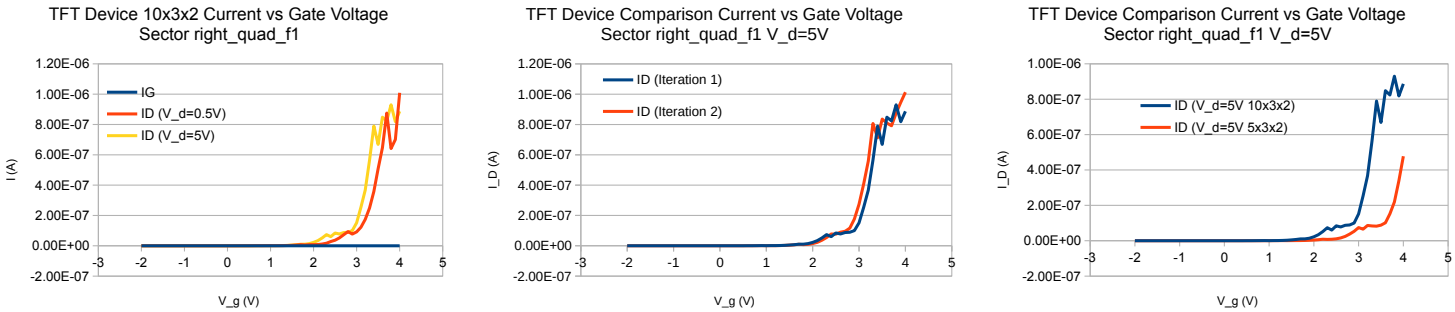

Fig. 3. Sample performance of individual devices when comparing against different V_{dd}, different sizes, and multiple runs, respectively. V_T tends to be around 2.5V regardless of configuration.

resistive materials, resistances, and TFT channel dimensions. A sample of these variations for NOTs are seen in Figure 1. The main metric we will focus on is finding the voltage transfer curves of each gate [4]. This involves varying each gate (input) voltage and measuring the output voltage. Finally, we created more complicated circuits for evaluation: AND (NOT+NAND), XOR, and a Flip Flop.

III. Results

In this section we present two classes of results: those from individual devices and those from logic gates. In our analysis, we were limited to four testing probes, which limits us to measuring one input and one output, after supplying source voltage V_{dd} and GND. This means that we are limited to testing simpler circuits, and also with only one input.

A. Individual Devices

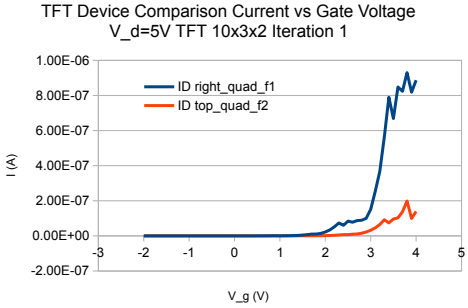

Fig. 4. Sample performance of individual devices when comparing against different sectors. Top quadrant device has a slightly higher V_T (2.5 vs 2.75V) but significantly lower peak current.

We plot the I-V (drain current vs input voltage) characteristics for We generally noted that a larger transistor produced steeper curve. Furthermore, repeated runs of the same device caused a leftward V_T shift. These results are shown in Figure 3.

We did notice wide variations across multiple sectors in device performance, which likely further affected results, which is seen in Figure 4 through the widely different peak current for the same gate voltage.

B. Logic Gates

We tested different variations of our circuits with different resistance materials (Tungsten or ITO), as well as varied the sizes of resistive material and TFT sizes. We test NOT, NAND, and NOR gates.

We analyze transfer characteristics of many devices. We see the results for a sample NOT gate in Figure 5. We note that having a lower Vdd provides poor results, with 5V giving clear results. Furthermore, larger transistor gives better gain. Note that the gain is not great, and turn on voltage very small positive

When checking across repeated runs, the consistency in the performance is not great. We see the threshold voltage shift left over multiple runs and eventually shift to a negative voltage. However, some sectors more affected than others. This is evident in Figure 7. We also noticed that the gain and peak current is increased by the introduction of light as seen in Figure 8.

We conducted cross-circuit transfer metrics which are presented in Figure 6. We do see better transfer characteristics with ITO pull-up resistors compared to Tungsten (W) resistors, which had a much lower gain. We demonstrates the transfer

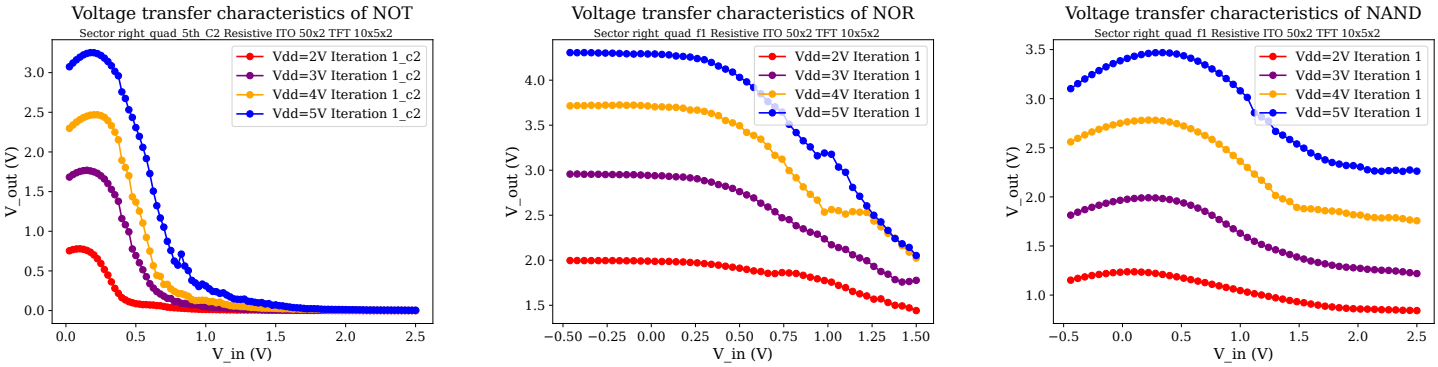

Fig. 5. Sample performance of NOT, NOR, and NAND gates across various V_{dd} input sweeps. Note that triggering the 2nd input gate for NOR and NAND produced similar results that are not shown. $V_T \approx 0.5V$ for sufficiently large V_{dd}. Gain is around 6 for NOT and 2 for NOR at $V_T = 0.5V$. NAND for a single on gate erroneously has 0.5 gain and $V_T = 0.5$.

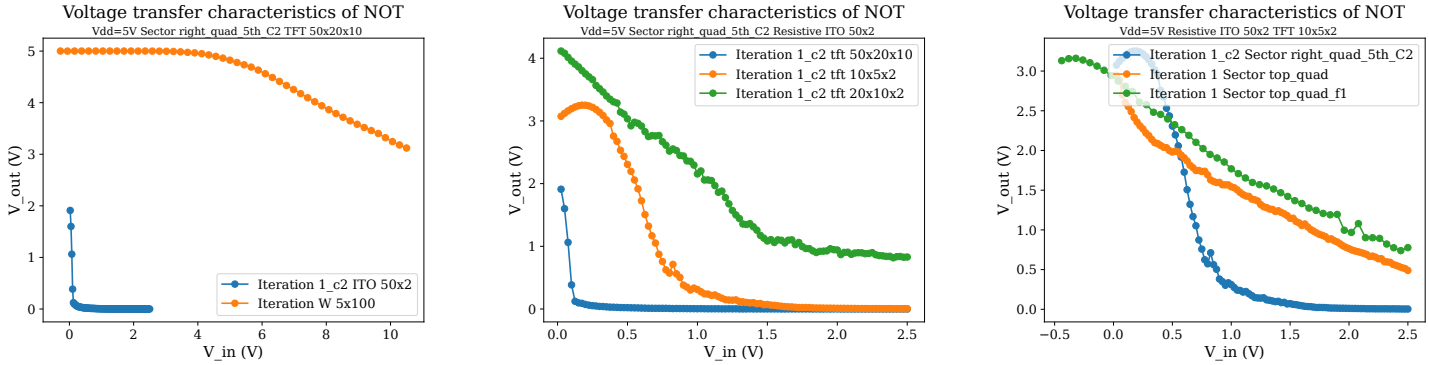

Fig. 6. Cross circuit comparisons: transfer performance by different resistive materials (ITO and W) in two different configurations, transfer performance by different TFT sizes, and transfer performance for the same circuit in different sectors. Tungsten devices had $V_T = 5V$ with gain of 0.5, while ITO devices had gain of 4 at $V_T = 0.25$. 50x20x10um (WxL_gxL_{ov}) TFT devices have a gain of 4 at V_T 0.25V, 10x5x2 have a gain of 6 at 0.5V, and 20x10x10 have a gain of 2 at 0.5V. Right quadrant devices saw gains of 4-6x higher.

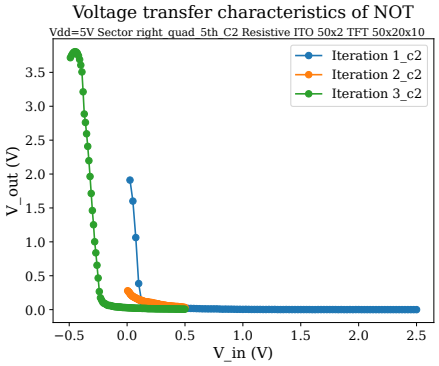

Fig. 7. Sample of how threshold voltage shifts left over multiple runs. We generally see a leftward shift in threshold voltage over many repetitions.

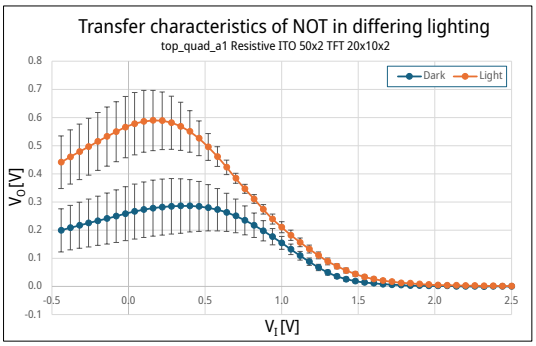

Fig. 8. Transfer characteristics of NOT got demonstrating the increase of output voltage in direct lighting lighting versus isolated from light. The measurements are on the same Resistive ITO of 50x2 and TFT of 20x10x2, both with constant drain voltage of 4 Volts.

characteristics of two circuits: one with a tungsten (5x100um) pull-up resistor and one with ITO (50x2um). The tungsten-based circuits turn on voltage was around 5-8V. These devices burnt before we could fully turn on (about 12V). We noted that 10x5x2um (W x Lg x Lov) TFTs produce higher gain and higher turn on voltage in general. We identified large differences between same circuits in different sectors. We found that circuits in the Right Quadrant C2 worked best with the best gain and best turn on voltage and were most consistent after many runs too.

IV. Theory

We model thin-film transistors (TFTs) as voltage-controlled resistive switches. When a high gate voltage is applied, the transistor turns ON and conducts with relatively low channel resistance but when it is pulled low, the channel becomes highly resistive [8].

In RTL circuits, the pull-up resistor connects the output node to the supply voltage (V_{DD}), while the transistor connects the output to ground. When the TFT gate is pulled high, the transistor turns on and pulls the output close to 0 V. When the gate is low, the transistor turns off, and the pull-up resistor pulls the output high [9] which forms the basis of an inverter and can be extended to make digital logic gates.

Ideally, we expect sharp voltage-transfer characteristics, particularly in the NOT and NOR gates. These should exhibit a steep gain (high dV_{out}/dV_{in}) around the threshold voltage V_T, resulting in a distinct switching point where the output rapidly transitions between logic levels [10]. This behavior is desirable for noise immunity and reliable digital operation. Our experimental results (see Figure 5) reflect this to some extent, with observable transitions near V_T, though the gain is not as sharp as we hoped. For NAND gates with only one gate input active, we expect the transistor network to remain conducting, holding the output at a high voltage. Understanding these individual device behaviors is essential for analyzing full circuit operation.

A. Discussion

We observe typical field-effect transistor behavior in the voltage transfer characteristics, with clear threshold voltages and typical behavior for different devices and logic circuits. When measuring the characteristics of both logic gates and individual devices, we got mixed performance results, with some producing great results, and others behaving in unexpected ways.

In our tests, we compared the results of two different device sizes. A larger transistor exhibited a lower turn-on voltage, which was unexpected as we anticipated that larger devices would require higher gate voltages due to increased channel area. With repeated runs, the threshold voltage shifted left, indicating poor process repeatability and limited reliability in the current fabrication setup. Comparing identical designs across different chip quadrants, we observed performance variation, suggesting that device location on the wafer impacts behavior, which further indicates fabrication defects in different sectors.

In an ideal case, we would expect turn-on gains of around 100. However, we saw gains ranging from 1-10. Devices in the right quadrant produced the best gains (about 6-8) with the other quadrants in the range of about 1-4. The NOT and NOR gates in the right quadrant produced these gains, indicating they can be used well as logic gates. We also observed a threshold voltage of about 0.25V in these gates. Furthermore, our NAND gate was not nearly as stable as expected, with a noticeable drop in voltage at V_T, and a gain of 1.

Similar to individual devices, we noticed that the across multiple runs, the threshold voltage slowly shifted left. We believe that this is caused by changes in the oxide layer when charge is applied. However, this meant that our threshold voltages would shift to be negative, rendering many circuits useless. We noticed that top quadrant devices were more affected as well by this issue, leading us to believe that imperfections in oxide deposition could have caused it as well as knowing the lift-off process partially failed.

When comparing by resistive material, ITO resistors produced better results with a higher gain and lower turn on voltage. When comparing by TFT size, 10x5x2um TFTs produced the best results with the best gain (~ 8. We believe that these variations are caused my mismatched on/off resistances of the TFTs with the pull-up resistance. We should in the future decrease the ITO resistor size and increase the W resistor size for better gains in stability.

We also compared a single device in both total darkness, making use of the light block on the probe station, and in direct light using the microscope light on the test bench. In direct lighting conditions we found that gain was higher than in dark conditions, as seen in Figure 8. We also saw that the voltage pickup before reaching the shutoff regime was steeper, thereby less consistent and more undesirable.

V. Conclusion

This project demonstrated the viability of using TFTs for basic digital logic in a research and prototyping context. Our results are promising. We are able to build relatively stable logic gates (NOT and NOR) with reasonable gain (about 20 at $V_T = 0.25V$). Further exploration should be in increasing the stability of our devices, by refining the fabrication, as well as testing larger circuits and exploring device/circuit variations near our expected 'best' sizes of 50x2um for ITO resistors and 10x5x2 for the TFTs to find the highest gain.

Our work confirms that this process for making TFTs, particularly when implemented with resistor-transistor logic (RTL), can form the building blocks of digital systems suited to large-area, low-cost, or flexible electronics.

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